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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/493,270	01/28/2000	Kazuyuki Shigeta	35C14208	2020

5514 7590 08/05/2003

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EXAMINER
ABDULSELAM, ABBAS I

ART UNIT	PAPER NUMBER
2674	6

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/493,270	SHIGETA, KAZUYUKI	
	Examiner	Art Unit	
	Abbas I Abdulselam	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 10-39 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) 1-9 is/are allowed.

6)☒ Claim(s) 10-39 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-9 are allowed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naka et al. (USPN 5990968) in view of Maeshima et al. (USPN 5389975) and Sasaki et al. (USPN 6430363).

Regarding claims 10-18 and 28, Naka teaches the video signal processing device (18) including input terminals (1, 2), a memory (6), RAM, which provides memory area for processing work of the micro-processor unit, MPU (9), a read out control circuit (8) and a D/A converting circuit (7), which enables the output video signals VO to the display (20) to become a signal subjected to predetermined image processing. Naka teaches that the MPU (9) can obtain data of any position on the screen from memory (6). Naka also teaches that the read out control circuit (8) controls the read-out order of the data from memory (6) and the selection of the read-out data from the memory (6) to read out the data so that an image represented by the data has a form corresponding to an instruction from MPU (9). See col. 5, lines 9-63, col. 6, lines 26-38 and Fig 2. In addition, Naka teaches a write control circuit (5) in terms of a loop filter (53) for

smoothing the output of a phase comparator (52) to acquire desired response characteristics. See col. 10, lines 32-50, and Fig 6. However, Naka does not teach the use of "at least one signal input units to which signals of a plurality of system are inputted'. Maeshima on the other hand teaches three way video inputs video 1, video 2 and video 3 that are provided to the input selection switch (1). See col. 2, lines 54-58 and Fg. 2.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify Naka's video signal processing system (Fig. 1) to adapt Maeshima's three way video inputting technique. One would have been motivated in view of the suggestion in Maeshima that the three way video inputting (video 1, video 2, video three) is functionally equivalent to the desired "inputting of plurality of systems". The use of three way inputting helps function a video information-identifying device more effectively as taught by Maeshima.

Naka does not teach synthesizing video signals of plurality of systems, and a control means selecting a preferential video signal according to image characteristics information of the videos signal of the plurality of systems.

Sasaki on the other hand teaches the use of television signals from a plurality of channels and synthesizing means for synthesizing the received television signals from plurality of channels into one screen. See col. 4, lines 37-45. For example, Sasaki illustrates the received video signals as input to the screen synthesizer (30) synthesizing the screens to arrive at synthesized video as shown on Fig 7. Sasaki further discloses the synthesized video as being "reproduced video" (see Fig. 8) from which only the video from the desired channel is retrieved and displayed on a TV monitor (13). See col. 15, lines 8-45, Fig. 5 and Fig (7-8).

Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify Naka's video signal processing device to include Sasaki's synthesizing means and technique of video signal selection as shown in Fig. 7 and Fig 8 respectively. One would have been motivated in view of the suggestion in Sasaki that the synthesizing means and video signal selection technique equivalently perform the desired functions of synthesizing video signals and selecting a preferential video signal respectively. The use of synthesizing means and video selection technique helps function a video signal recording apparatus more effectively as taught by Sasaki et al.

With respect to claims 11 and 16, in addition to what has been described, Naka teaches a display (20) in conjunction with controlling the display video signal generator (19) to output the video signals VI representing the stored pattern subject to the adjustment of the sampling clock. See col. 4, lines 40-49 and Fig 1.

With respect to claims 12 and 17, in addition to what has been described, Naka teaches a communication terminal (16) for inputting the control signal from the external controller (21) into the MPU (9). See col. 16, lines 61-63.

With respect to claims 13 and 18, in addition to what has been described, Naka teaches the video signal processing device (18) adjusting the video signals (VI) after which the device performs image processing on the video signals (VI), representing any picture which is output from generator (19) and then outputs the video (VO) signals to the display (20). See col. 4, lines 61-67, col. 5, lines 1-5 and Fig 1.

With respect to claims 14-15, in addition to what has been described above, Naka teaches the MPU (9) obtaining data of any position on the screen from the memory (6) and further

teaches a correction on the screen, which involves optimizing the sampling clock phase with the data corresponding to the picture elements on the screen.

With respect to claim 28, in addition to has been described, Naka teaches that by controlling the write-in control circuit (5) with the phase control signal CKPH, the phase of the sampling clocks can be adjusted in order to ultimately achieve picture elements that maintain the image quality. See col.11, lines 27-38. Naka also teaches an output terminal (12, 17), and a communication terminal (16) for inputting the control signal in terms of phase adjustment. See col. 5, lines 48-62.

Regarding claim 32, Naka teaches a phase adjustment with respect to the sampling clock phase for all the video signals which are possibly input and vary set values in accordance with the change of the input video signals. See col. 2, lines 25-34. In addition, Naka teaches generating the sampling of clocks in terms of a divider (55) which is reset by the signal V so that the phase relationship between the signal, V and the sampling clock is kept fixed at all times. See col. 10, lines 62-65.

Regarding claims 19-20 and 25, Naka teaches a signal as an input from the video signal generator (19) into the video inputting device (18) where the optimum adjustment amount obtained is stored in the non-volatile memory (22) for every video signal. See col. 11, lines 55-67.

Regarding claims 21-23, Naka teaches timing charts showing the variation of sampling data with sampling clock phase. See Fig 3(A-E).

Regarding claims 24 and 26, Naka teaches the video signal-processing device (18) with respect to signals with improved resolution. See col. 17, lines 13-22.

Regarding claim 27, Naka teaches a video signal generator (19) inputting video signals with a test pattern of having two gradation levels, 0% brightness (black signal) and 100 % brightness (white signal).

Regarding claims 29-31, Naka teaches a video signal processing device adjusting the sampling clocks by determining a correction direction of the phase of a sampling clocks though means of calculations. See col. 2, lines 40-65. Moreover, Sasaki teaches a system controller (16) setting the tuner (2) to respective channels (Fig. 6) in accordance with information supplied from the timer (17) such that the electric waves for a given channel are selected from the electric waves received by antenna (1), and the demodulator (3) demodulates the received waves into signals. See col. 6, lines 35-47.

Regarding claims 33-39, Naka teaches the processing device (18) including its internal constructions, used with a display (20) which can be of any kind of workstations or computers Fig 1, Fig 2 and col. 18, lines 43-55. Sasaki also teaches the use of television monitor (13) as shown in Fig 1.

Conclusion

3. The prior art made of record and not relied upon is considered to applicant's disclosure. The following arts are cited for further reference.

U.S. Pat. No. 5,260,905 to Mori

U.S. Pat. No. 5,473,414 to Hayashi et al.

U.S. Pat. No. 5,767,865 to Inoue et al.

U.S. Pat. No. 6,049,360 to Yanai et al.

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulselam** whose telephone number is **(703) 305-8591.** The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709.**

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand delivered responses should be brought to Crystal Park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

Abbas Abdulselam

Examiner

Art Unit 2674

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600